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first and second insulation-filled trench regions having an outer layer of doped silicon material which is discontinuous along a bottom surface of the insulation-filled trench region so that the insulation material along the bottom surface of the insulation-filled trench region is in direct contact with the first semiconductor region, the outer layer of silicon material being of a conductivity type opposite that of the first semiconductor region; and

- a termination structure comprising an insulation-filled termination trench region extending from the first surface into the first semiconductor region, the termination trench region being laterally spaced from the first and second trench regions so that during an operating mode of the field effect transistor a substantially uniform electric field in the region between the termination trench region and the first and second trench regions is obtained.

**15.** The field effect transistor of claim **14** wherein the insulation-filled termination trench region includes an outer layer of doped silicon material which is discontinuous along

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a bottom surface of the insulation-filled trench region so that the insulation material along the bottom surface of the insulation-filled trench region is in direct contact with the first semiconductor region.

**16.** The field effect transistor of claim **2** wherein the gate trench region further includes:

a gate dielectric lining sidewalls of the gate trench region; and

a thick bottom dielectric filling a bottom portion of the gate trench region below the gate.

**17.** The field effect transistor of claim **6** wherein the first and second insulation-filled trench regions are spaced apart in the first semiconductor region to form a drift region therebetween, the volume of each of the first and second insulation-filled trench regions being greater than one-quarter of the volume of the drift region so as to reduce output capacitance and improve thermal performance of the field effect transistor.

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